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(54) ATM queuing and scheduling apparatus

(57) The apparatus is used for queuing and scheduling ATM cells across an ATM switch. A sustainable cell rate calendar is connected in series with a peak cell rate calendar and cells are scheduled independently in each. The sustainable cell rate calendar guarantees the maximum ATM cell delay is not exceeded. The ATM cells are

not placed on the peak cell rate calendar unless the peak cell rate threshold might be exceeded. In this case the cell is scheduled on the peak cell rate calendar and it is this that determines when the cell is sent. In this way, it is possible to guarantee absolute minimum and maximum cell rates of a connection.

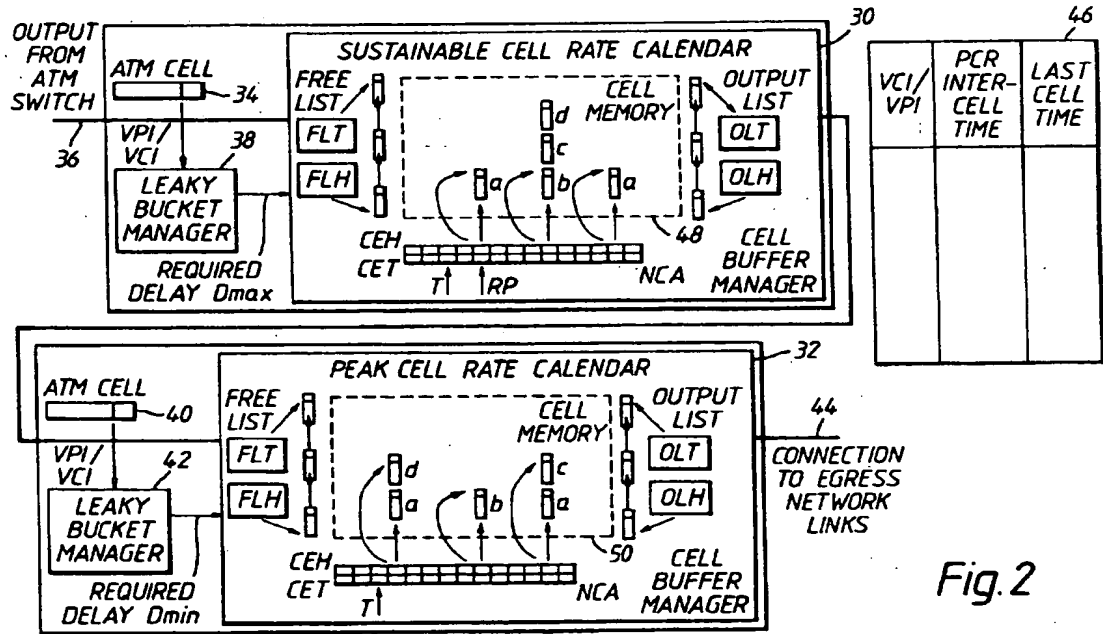


Fig. 2

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Description

The present invention relates to apparatus for queuing and scheduling ATM cells in an ATM switch.

ATM networks and switches support a mixture of traffic including bursty traffic. By its nature, bursty traffic requires high bit rates for part of the time and little or no bit rate for the rest of the time. In order to use efficiently the bit rate available in a network, it is necessary to allocate a connection at a lower bit rate than the peak bit rate, such that the total peak bit rate of all the connections may be greater than the bit rate of the network links.

In a German Patent Application No 93120828.4, there is detailed a method of providing an output of ATM cells whereby the sustainable cell rate as defined in the ATM Forum User Network Interface (UNI) specification, version 3.0, is guaranteed. By using a leaky bucket method, as described in the ATM Forum UNI specification, version 3.0, each ATM cell has the time of transmission from the system calculated by identification of its virtual channel identifier/virtual path identifier (VCI/VPI) field, or other similar method which uniquely identifies ATM cells belonging to the same communication connection. This transmission time is provided as a delay value and is used to schedule the ATM cell on a calendar, which is effectively a time scheduler.

The problem with the method as mentioned in this German patent application, is that it does not limit the minimum delay, ATM cells can be transmitted at up to the maximum bit rate of the network link. This means that the cells can exceed the peak cell rate (PCR) of the connection as defined in the ATM Forum UNI specification, version 3.0.

In GB Patent Application No 9405788.2, another method is disclosed which uses two calendars. The first calendar, as with the above mentioned German patent application, guarantees the sustainable cell rate, by scheduling ATM cells according to the sustainable cell rate leaky bucket delay value. This calendar is called the sustainable cell rate (SCR) calendar. A second calendar is used which limits the peak cell rate. The second calendar is called the peak cell rate (PCR) calendar and schedules the cells according to their PCR delay value. Although there are two calendars, each ATM cell is stored only once. Each ATM cell is pointed to from both calendars. The second calendar has some distinct differences in the way it operates as follows:

The SCR calendar has two time pointers, a real time read pointer (T) and a read pointer (RP).

The PCR calendar has only one pointer, a real time read pointer (T).

The SCR calendar read pointer will move from one filled time slot to the next filled time slot. For both SCR and PCR calendars the real time read pointer will only move by one time slot each ATM cell transmission period.

Once the real time read pointer of the PCR calendar has passed a time slot, it will remove the pointer from the ATM cell, returning it to a null value. This is the key for

the SCR calendar to transmit the cell from the system when it arrives.

The system is intended to limit the ATM cell rate for a specific connection to within its specified threshold for the sustainable cell rate and the peak cell rate, that is the maximum and minimum ATM cell rate.

There is a problem with the above mentioned prior art system, in that, in a specific situation it is possible that the peak cell rate may exceed the PCR value set. This occurs if there is sudden change in the usage of the system from high to low usage.

In a high load situation, the real time read pointer moves from cell slot to cell slot removing the PCR pointer from cells. However, the cells are actually transmitted from the system based on the read pointer, which in a high load situation will operate as a slow rate. It is possible that the real time read pointer on the PCR calendar may remove the PCR pointer from several ATM cells all belonging to the same connection before the read pointer of the SCR calendar sends them. If the system enters a low load period, the read pointer will run faster and send any ATM cells with a null PCR pointer. There is therefore the opportunity to send ATM cells from the same connection at a greater ATM cell rate than the PCR value.

An aim of the present invention is to provide ATM queuing and scheduling apparatus which does not suffer from the above mentioned problem.

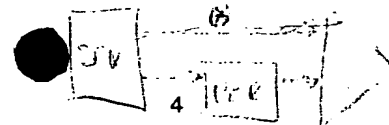
According to the present invention there is provided apparatus for queuing and scheduling ATM cells connected to an output side of an ATM switch, comprising first and second calendars connected in series, said first calendar being used to schedule cells for transmission in accordance with a maximum delay value, said second calendar being used to schedule cells for transmission in accordance with a minimum delay value, and comparator means for determining when a cell is to be scheduled on said second calendar.

An embodiment of the present invention will now be described with reference to the accompanying drawings, in which,

FIGURE 1 shows a block diagram of a typical ATM switch,

and,
FIGURE 2 shows a sustainable bit rate calendar and a peak bit rate calendar connected in series, together with a table which is used to identify the VCI/VPI, the PCR intercell time and the last cell time.

Referring to Figure 1, on the ingress side are shown line cards 8, the output of which are connected to an input of an ATM multiplexer 12. The output of the multiplexer 12 is connected to an input of a statistical multiplexing unit 16, the output of which is fed to the ATM switching network 20. The output of the switching network 20 is connected to an input of a further statistical multiplexing unit 18, the output of which is connected to an input of an ATM multiplexer 14. The outputs of the ATM multi-



plexer 14 are connected to the input of a number of line cards 10 which are on the egress side of the switching network. The links between the various components designated M represent multiplexed internal links. Each statistical multiplexing unit has a flow control controller 22. The combination, for example, of the line cards 8, multiplexer 12 and statistical multiplexing unit 16 comprises a peripheral switch group. In practice there will be a number of peripheral switch groups connected to the ATM switching network. Within each statistical multiplexing unit 16 there is one input queue for each of the peripheral switch groups attached to the ATM switching network. Cells may be sent independently between any of the peripheral switch groups. There are limiting factors which control the cell rate, and they are the output link bit rate from the ATM switching network to a peripheral switch group, and the output link bit rate from a peripheral switch group to the ATM switching network.

Flow control procedures operate to manage these limited bit rates fairly for all connections, both internally to the switch and between the peripheral switch groups, and to limit bit rate to peak reservation across the ATM switching network.

The present invention is conveniently located in the statistical multiplexing unit 18 and will now be described.

Referring to Figure 2, there is shown a sustainable bit rate calendar 30 serially connected to a peak bit rate calendar 32. ATM cells 34 are received over a line 36 from the ATM switch of Figure 1, and are processed by a leaky bucket manager circuit 38, which is used to generate the required maximum delay D_{max} . The ATM cells 40 which are fed out from the sustainable bit rate calendar 30, are processed by a leaky bucket manager circuit 42, to provide the required minimum delay D_{min} .

In Figure 2, the following abbreviations are used, FLT is the Free List Tail, FLH is the Free List Head, CET is the Calendar Entry Tail, CEH is the Calendar Entry Head, RP is the Read Pointer, T is the Real Time Pointer, OLT is the Output List Tail, OLH is the Output List Head, MCA is the Size of Calendar, VPI is the Virtual Path Indicator, VCI is the Virtual Channel Indicator.

In Figure 2 there is also shown a table 46, in which would be listed the VCI/VPI data which identifies the ATM cell address, the PCR intercell time, which represents the peak cell rate intercell time, and a further column identified as last cell time.

By placing the two calendars 30, 32 in series, cells A to D for example, may be scheduled independently in each calendar in their respective cell memory 48, 50 in accordance with the read pointer of RP and the real time pointer T.

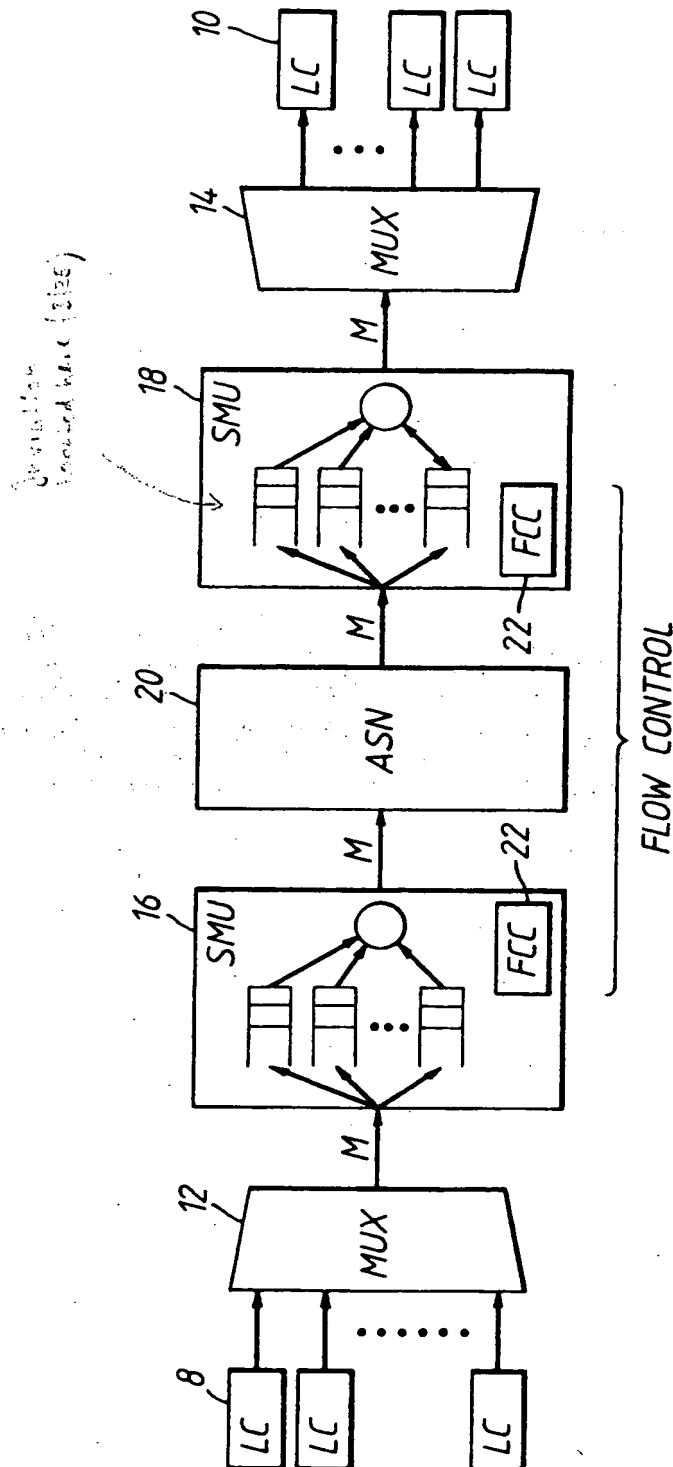
In operation, cells leaving the sustainable cell rate calendar 30 are checked against the table values for the peak cell rate intercell time and the last time a cell was transmitted. If the intercell time will be less with this particular cell being transmitted immediately, the cell must be scheduled on the peak cell rate calendar 32 at an intercell time. The sustainable cell rate therefore guarantees the maximum ATM cell delay is not exceeded. The

ATM cells are not placed on the peak cell rate calendar 32 unless the above mentioned PCR threshold might be exceeded. It is the scheduling on the peak cell rate calendar which determines when the cell is sent. In this manner it is possible to guarantee absolutely the minimum and maximum cell rate of a connection is observed.

It will be readily appreciated that there are various ways of implementing the control of the sustainable cell rate calendar and the peak cell rate calendar which fall within the scope of the present invention.

Claims

1. Apparatus for queuing and scheduling ATM cells connected to an output side of an ATM switch, comprising first and second calendars connected in series, said first calendar being used to schedule cells for transmission in accordance with a maximum delay value, said second calendar being used to schedule cells for transmission in accordance with a minimum delay value, and comparator means for determining when a cell is to be scheduled on said second calendar.
2. Apparatus as claimed in Claim 1, wherein said apparatus comprises buffer means connected to an input line upon which ATM cells are received, first control means for receiving for each cell a channel identifier and a path identifier from which a first signal is generated indicative of said maximum delay value, said first calendar in which said cell is scheduled for transmission in accordance with the maximum delay value being used to control a sustainable cell rate, an output line from said first calendar which is connected to an input of said second calendar, second buffer means for receiving ATM cells from said first calendar, and second control means for receiving a channel identifier and a path identifier in respect of the received cell for generating a second signal indicative of said minimum delay value, which is used to schedule the particular cell for transmission on said second calendar for controlling a peak cell rate, wherein, cells are dispatched from said first calendar and are compared by said comparator means against a table of values for a peak cell rate intercell time and a last time the particular cell was transmitted and if said intercell time will be less when said cell is transmitted immediately, said cell is scheduled on said second calendar at said intercell time.



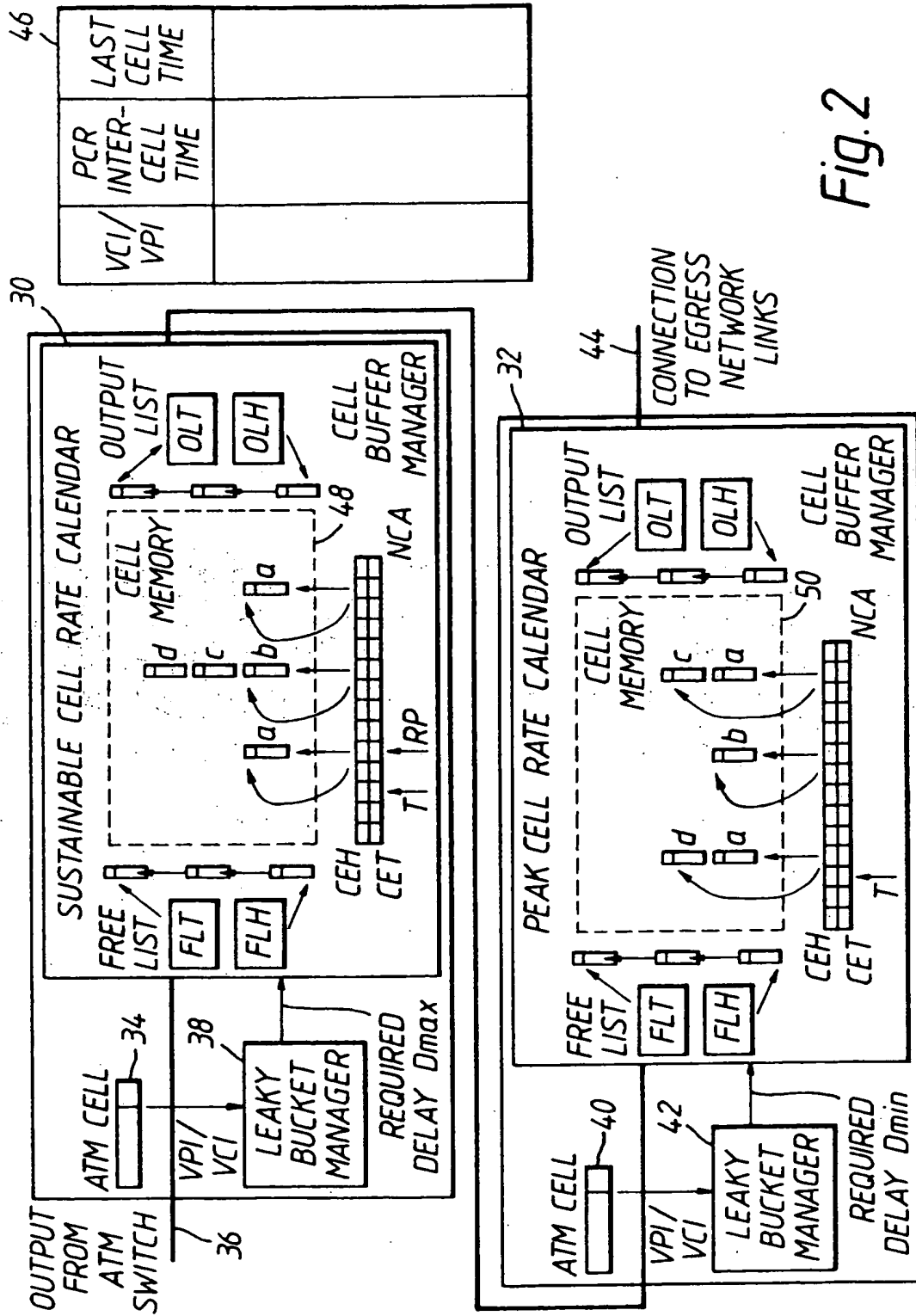


Fig. 2

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